Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT 2**
2. **OUTPUT 1**
3. **VCC**
4. **–INPUT 1**
5. **+INPUT 1**
6. **–INPUT 2**
7. **+INPUT 2**
8. **–INPUT 3**
9. **+INPUT 3**
10. **–INPUT 4**
11. **+INPUT 4**
12. **GND**
13. **OUTPUT 4**
14. **OUTPUT 3**

**.040”**

**.040”**

**2 1 14 13**

**MASK**

**REF**

**3**

**4**

**5**

**6**

**7 8**

**12**

**11**

**10**

**9**

**U439**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref: U439**

**APPROVED BY: DK DIE SIZE .042” X .042” DATE: 11/2/21**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: LM139A**

**DG 10.1.2**

#### Rev B, 7/1